DATA SHEET

PCA9515
I²C bus repeater

Product data
Supersedes data of 2002 Mar 01

2002 May 13

Philips
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I²C bus repeater PCA9515

DESCRIPTION

The PCA9515 is a BiCMOS integrated circuit intended for application in I²C and SMBus systems.

While retaining all the operating modes and features of the I²C system it permits extension of the I²C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515 enables the system designer to isolate two halves of a bus, thus more devices or longer length can be accommodated. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other is required.

FEATURES

- 2 channel, bi-directional buffer
- I²C-bus and SMBus compatible
- Active high repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates standard mode and fast mode I²C devices and multiple masters
- Powered-off high impedance I²C pins
- Operating supply voltage range of 3.0 V to 3.6 V
- 5 V tolerant I²C and enable pins
- 0 to 400 kHz clock frequency[1]
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA.
- Package offerings: SO and TSSOP

PIN CONFIGURATION

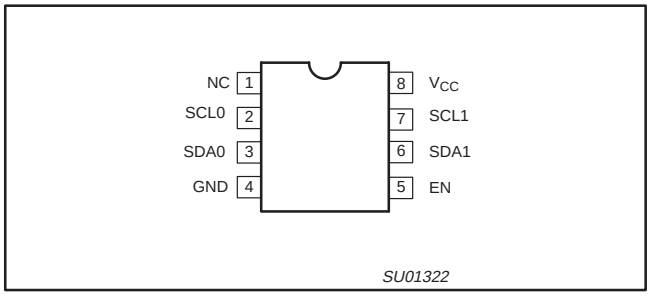


Figure 1. Pin configuration

PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1	NC	No connection
2	SCL0	Serial clock bus 0
3	SDA0	Serial data bus 0
4	GND	Supply ground
5	EN	Active high repeater enable input
6	SDA1	Serial data bus 1
7	SCL1	Serial clock bus 1
8	V_{CC}	Supply power

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
8-pin plastic SO	–40 to +85 °C	PCA9515D	SOT96-1
8-pin plastic TSSOP	–40 to +85 °C	PCA9515DP	SOT505-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

1. The maximum system operating frequency may be less than 400 KHz because of the delays added by the repeater.

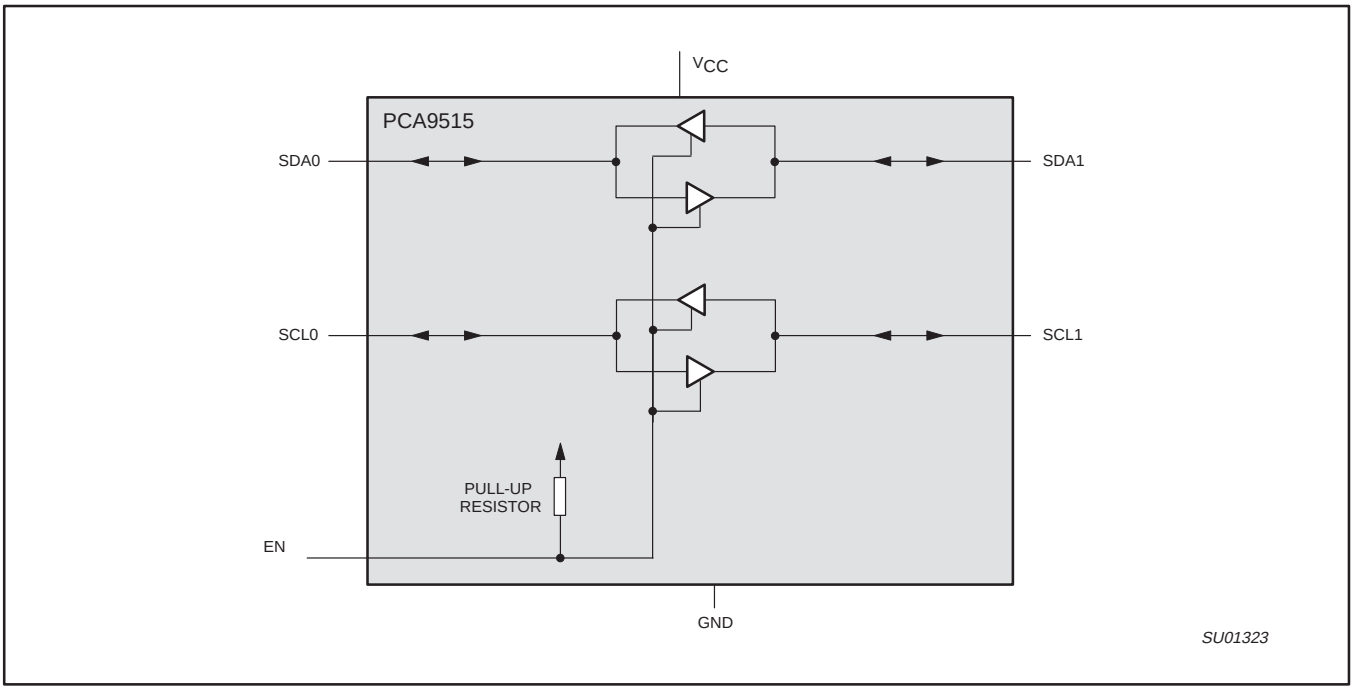


Figure 2. Block Diagram: PCA9515

The output pull-down of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven low. This prevents a lock-up condition from occurring.

FUNCTIONAL DESCRIPTION

The PCA9515 BiCMOS integrated circuit contains two identical buffer circuits which enable I²C and similar bus systems to be extended without degradation of system performance.
The PCA9515 BiCMOS integrated circuit contains two bi-directional, open drain buffers specifically designed to support the standard low-level-contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9515 acts like a pair of non-inverting, open drain buffers, one for SDA and one for SCL.

Enable

The EN pin is active high with an internal pull up and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power up until after the system power up reset. It should never change state during an I²C operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

I²C Systems

As with the standard I²C system, pull-up resistors are required to provide the logic HIGH levels on the Buffered bus. (Standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with standard mode and fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I²C system where standard mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used. Please see Application Note AN255 *"I²C & SMBus Repeaters, Hubs and Expanders"* for additional information on sizing resistors and precautions when using more than one PCA9515/PCA9516 in a system or using the PCA9515/16 in conjunction with the P82B96.

APPLICATION INFORMATION

A typical application is shown in Figure 3. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

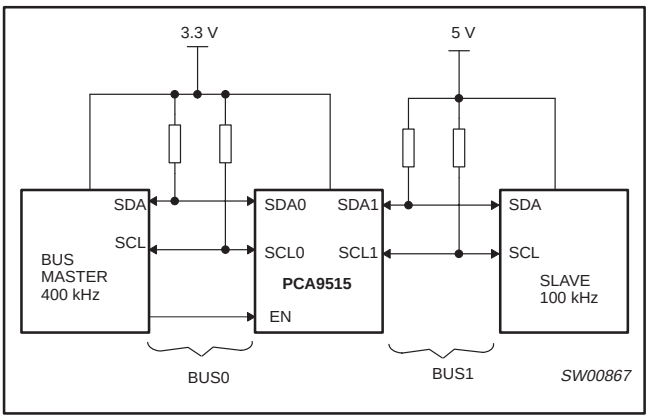


Figure 3. Typical application

The PCA9515 is 5 V tolerant so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515 is pulled low by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side to also go low. The side driven low by the PCA9515 will typically be at V_{OL} = 0.5 V.

In order to illustrate what would be seen in a typical application, refer to Figure 4 and 5. If the bus master in Figure 3 were to write to the slave through the PCA9515, we would see the waveform shown in Figure 4 on Bus 0. This looks like a normal I²C transmission until the falling edge of the 8th clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9515. Because the V_{OL} of the PCA9515 is typically around 0.5 V, a step in the SDA will be seen. After the master has transmitted the 9th clock pulse, the slave releases the data line.

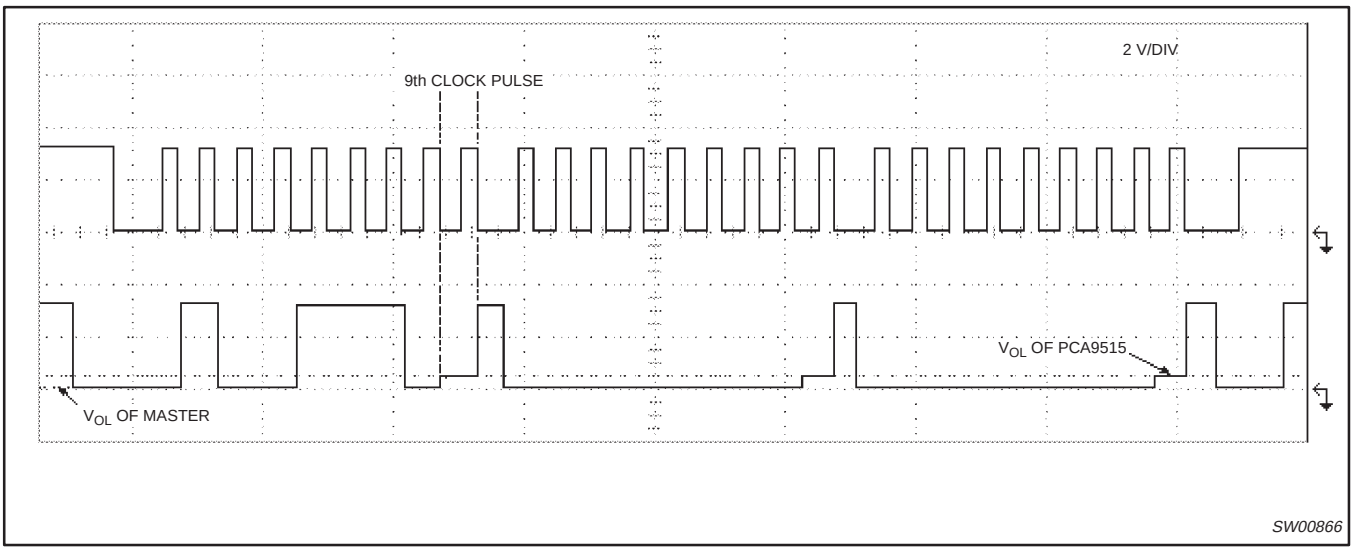


Figure 4. Bus 0 waveform

On the Bus 1 side of the PCA9515, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9515. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device that is very close to ground in our example.

It is important to note that any arbitration or clock stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PCA9515 (see $V_{OL} – V_{ilc}$ in the DC Characteristics section) to be recognized by the PCA9515 and then transmitted to Bus 0.

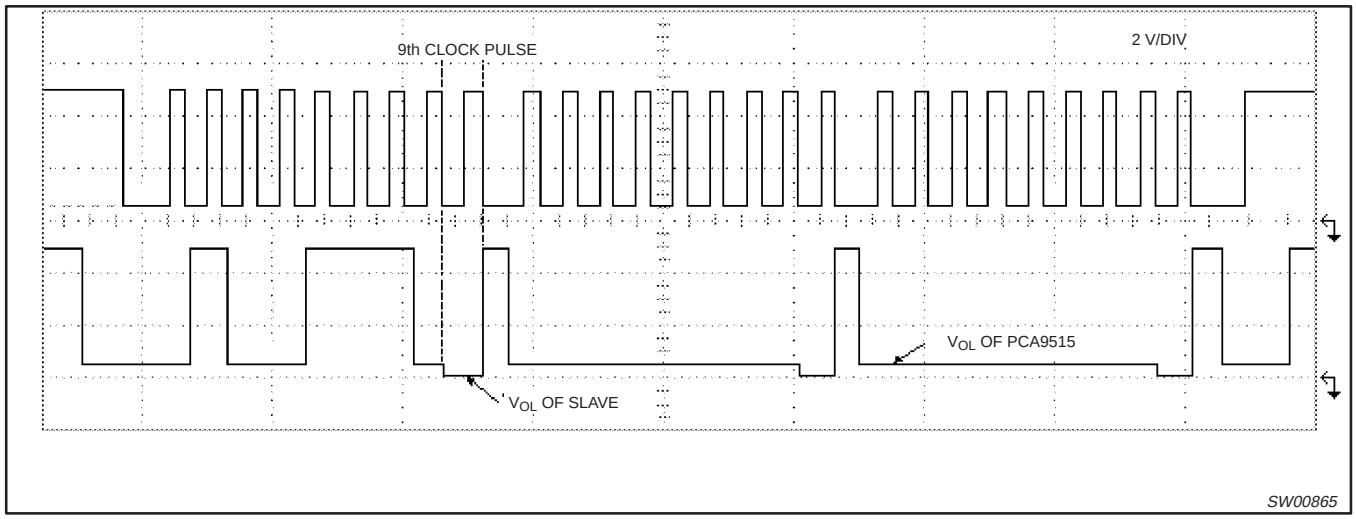


Figure 5. Bus 1 waveform

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	–0.5	+7	V
V_{bus}	Voltage range I^2C-bus, SCL or SDA	–0.5	+7	V
I	DC current (any pin)	—	50	mA
P_{tot}	Power dissipation	—	100	mW
T_{stg}	Storage temperature range	–55	+125	°C
T_{amb}	Operating ambient temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0 to 3.6 V; GND = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supplies						
V_{CC}	DC supply voltage		3.0	3.3	3.6	V
I_{CCH}	Quiescent supply current, both channels HIGH	V_{CC} = 3.6 V; SDAn = SCLn = V_{CC}	—	2.3	5	mA
I_{CCL}	Quiescent supply current, both channels LOW	V_{CC} = 3.6 V; one SDA and one SCL = GND, other SDA and SCL open	—	2.3	5	mA
I_{CCLc}	Quiescent supply current in contention	V_{CC} = 3.6 V; SDAn = SCLn = GND	—	2.1	5	mA
Input SCL; input/output SDA						
V_{IH}	High-level input voltage		0.7 V_{CC}	—	5.5	V
V_{IL}	Low-level input voltage (Note 1)		–0.5	—	0.3 V_{CC}	V
V_{ILc}	Low-level input voltage contention (Note 1)		–0.5	—	0.4	V
V_{IK}	Input clamp voltage	I_I = –18 mA	—	—	–1.2	V
I_I	Input leakage current	V_I = 3.6 V	—	—	±1	µA
I_{IL}	Input current LOW, SDA, SCL	V_I = 0.2 V, SDA, SCL	—	—	10	µA
V_{OL}	Low level output	I_{OL} = 0 or 6 mA	0.47	0.52	0.6	V
V_{OL}–V_{ILc}	Low level input voltage below output low level voltage	Guaranteed by design	—	—	70	mV
I_{OH}	Output high level leakage current	V_O = 3.6 V	—	—	10	µA
C_I	Input capacitance	V_I = 3 V or 0 V	—	6	7	pF
Enable						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{IL}	Input current LOW, EN	V_I = 0.2 V, EN	—	10	30	µA
I_{LI}	Input leakage current		–1	—	1	µA
C_I	Input capacitance	V_I = 3.0 V or 0 V	—	6	7	pF

NOTE:
1. V_{IL} specification is for enable input and the first low level seen by the SDAx/SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx/SCLx lines.

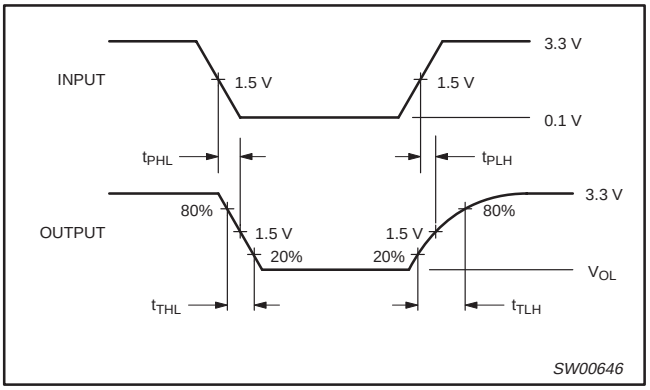
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
t_{PHL}	Propagation delay	Waveform 1	57	98	170	ns
t_{PLH}	Propagation delay	Waveform 1	33	55	78	ns
t_{THL}	Transition time	Waveform 1	—	67	—	ns
t_{TLH}	Transition time	Waveform 1; Note 1	—	135	—	ns
t_{SET}	Enable to Start condition		100	—	—	ns
t_{HOLD}	Enable after Stop condition		100	—	—	ns

NOTE:

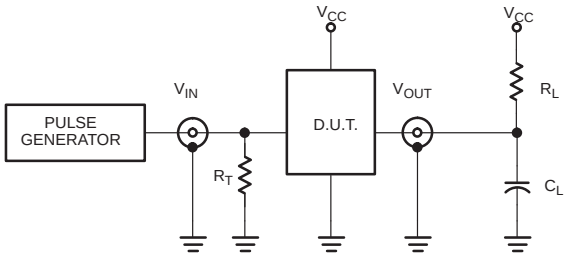
1. The t_{TLH} transition time is specified with loads of 1.35 kΩ pull-up resistance and 7 pF load capacitance, plus an additional 50 pF load capacitance. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

AC WAVEFORMS



Waveform 1.

TEST CIRCUIT



Test Circuit for Open Drain Outputs

DEFINITIONS

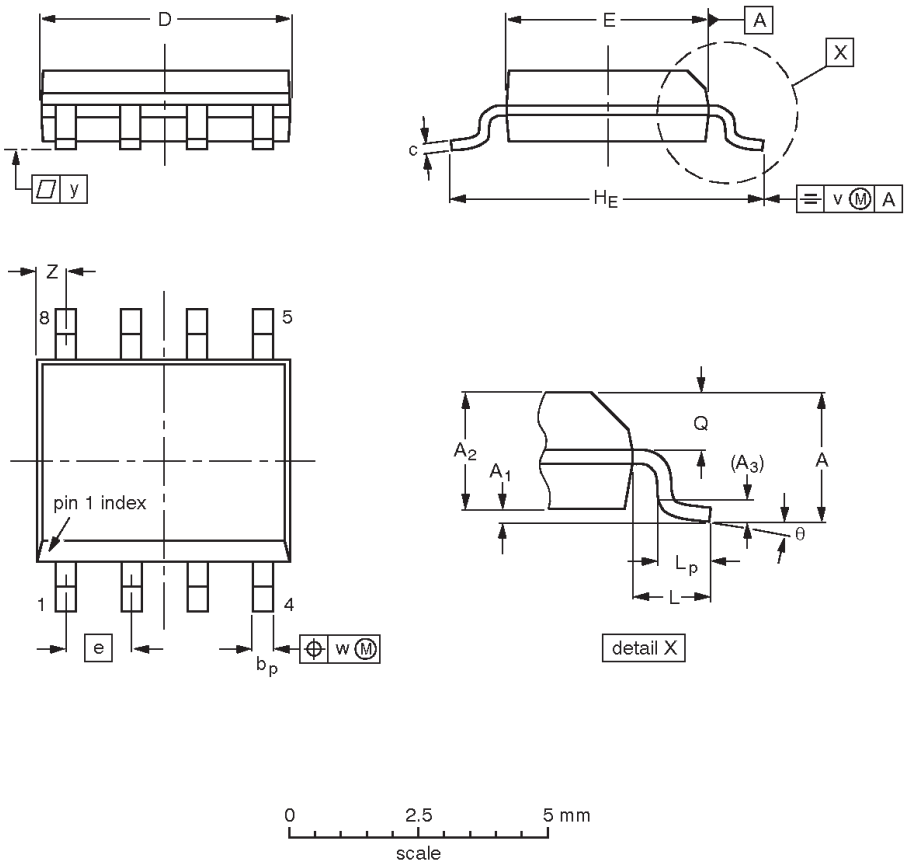
R_L = Load resistor; 1.35 kΩ

C_L = Load capacitance includes jig and probe capacitance; 7 pF

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00792

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

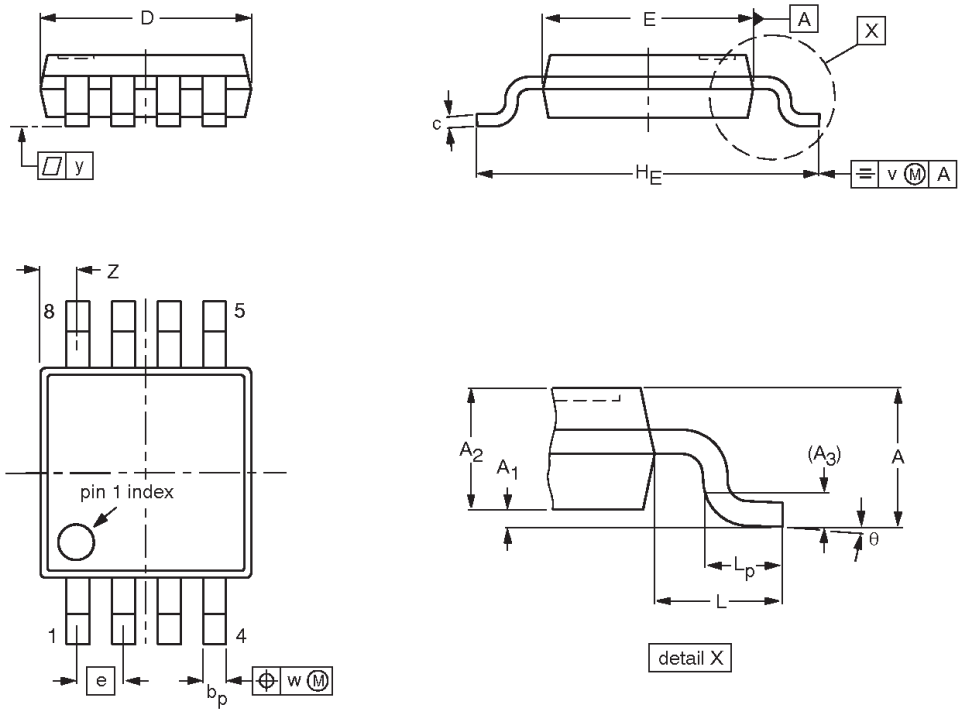
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

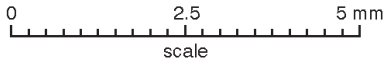
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

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2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

I²C bus repeater PCA9515

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Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 05-02

Document order number: 9397 750 09814

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